

13. The method of claim **12**, wherein the average width of the sections of the source element is less than about 10 microns.

14. The method of claim **12**, wherein a source electrode is configured to couple a source current segment through vias to a plurality of source elements distributed along the source electrode.

15. The method of claim **12**, further comprising insulating the source electrodes from the drain elements and insulating the drain electrodes from the source elements.

16. The method of claim **12**, further comprising removing heat from the source element and the drain element through the source electrode and the drain electrode.

17. The method of claim **12**, wherein the Field Effect Transistor is fabricated using gallium arsenide or gallium nitride.

18. A means for switching current using a Field Effect Transistor comprising:

means for segmenting source current;

means for distributing segments of the segmented source current to sections of a source finger disposed on a surface of a gallium arsenide compound semiconductor;

means for segmenting drain current;

means for distributing segments of the segmented drain current to sections of a drain finger disposed on the surface of the gallium arsenide; and

means for coupling a gate signal to two ends of a gate finger disposed between the source element and the gate element.

19. The means for switching current of claim **18**, further comprising a plurality of electrodes each configured to conduct a segment of the source current to a section of the source finger through a via.

20. The means for switching current of claim **19**, further comprising a dielectric layer between the plurality of electrodes and the source finger, the dielectric layer configured to embed the via.

21. The means for switching current of claim **18**, further comprising at least one via disposed on the surface of each section of the source finger.

22. The means for switching current of claim **18**, wherein the average width of the sections of the source finger is less than about 20 microns.

23. The means for switching current of claim **18**, wherein the means for coupling a gate signal to two ends a gate finger includes a first gate pad coupled to the gate signal and to a first

end of the gate finger, and a second gate pad coupled to the gate signal and to a second end of the gate finger.

24. A Field Effect Transistor device comprising:

a compound semiconductor layer a plurality of source fingers disposed on a surface of the semiconductor layer;

a plurality drain fingers disposed on the surface of the semiconductor layer and alternating with the source fingers;

a plurality of gates disposed between adjacent source fingers and drain fingers;

a plurality of first gate pads each configured to couple a gate signal to a first end of at least one of the gate fingers;

a plurality of second gate pads each configured to couple the gate signal to a second end of at least one of the gate fingers;

a dielectric layer disposed on the source fingers, drain fingers and gate fingers;

a plurality of source electrodes disposed on the dielectric layer along a width of the source fingers and oriented to cross the plurality of source fingers, each electrode electrically coupled through at least one via in the dielectric layer to a section of each of the source fingers; and

a plurality of drain electrodes disposed on the dielectric layer along a width of the drain fingers and oriented to cross the plurality of drain fingers, each electrode electrically coupled through at least one via in the dielectric layer to a section of each of the drain fingers.

25. The Field Effect Transistor device of claim **24**, wherein the length of each of the plurality of gate fingers is less than about 0.5 microns.

26. The Field Effect Transistor device of claim **24**, wherein the length of each of the plurality of source fingers is less than about 7 microns.

27. The Field Effect Transistor device of claim **24**, wherein the pitch of the gate fingers is less than about 15 microns.

28. The Field Effect Transistor device of claim **24**, wherein the compound semiconductor is gallium arsenide or gallium nitride.

29. The Field Effect Transistor device of claim **24**, wherein the sum of the widths of the gate fingers is greater than 1.0 meters.

30. The Field Effect Transistor device of claim **24**, wherein the a pitch of the source electrodes is less than about 30 microns.

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